REMARKS

In accordance with the foregoing, claims 1 and 4 are amended and new claims 6 and 7 are presented. No new matter is being presented, and approval and entry are respectfully requested.

Claims 1-7 are pending and under consideration. Reconsideration is respectfully requested.

Item 2 of the Office Action states "This application current names joint inventors." Applicant respectfully points out that the current application does not currently name joint inventors, and correction reflecting the same is requested.

Claim Amendments

Claim 1 is amended to recite transmission equipment transmitting traffic signals including "an input traffic collector which collects and retains a traffic amount of traffic signals input in each input port . . . ; a bandwidth set processor which calculates a bandwidth for use in each input port from the traffic amount of traffic signals . . . , calculates a corresponding number of virtual concatenation member paths from a difference between the calculated bandwidth in use and a virtual concatenation path bandwidth having been allocated to the input port, and issues an addition command for adding or a deletion command for deleting the virtual concatenation member paths for the calculated number; a virtual concatenation controller which sets a virtual concatenation path bandwidth on the traffic input from the plurality of ports; and a link capacity adjustment scheme controller which controls the virtual concatenation to set and change the virtual concatenation path bandwidth, . . . " Amendatory language being underlined. Dependent claim 4 is amended to correspond to parent claim 1.

Support for the amendents is found, for example, on page 14, line 15 - page 16, line 20. paragraphs. No new matter is being presented, and approval and entry are respectfully requested.

Traverse of Rejections under 35 U.S.C. §103

In item 3 of the Office Action, the Examiner rejects claim 1 under 35 U.S.C. §103(a) as being unpatentable over Acharya (U.S.P. App. Pub. 2004/0252633) in view of Sandstrom (U.S.P. 6,697,373). This rejection is traversed and reconsideration is requested.

Independent claim 1, as amended herein, recites:

a) "an input traffic collector which collects and retains a traffic amount of traffic signals input in each input port for one period at preset periods;"

b) "a bandwidth set processor which calculates a bandwidth for use in each input port from the traffic amount of traffic signals, retained in the input traffic collector, calculates the corresponding number of virtual concatenation member paths from the difference between the calculated bandwidth in use and a virtual concatenation path bandwidth having been allocated to the input port, and issues an addition command for adding or a deletion command for deleting the virtual concatenation member paths for the calculated number;"

c) "a virtual concatenation controller which sets a virtual concatenation path bandwidth on the traffic input from the plurality of ports; and

d) "a link capacity adjustment scheme controller which controls the virtual concatenation to set and change the virtual concatenation path bandwidth, based on the addition command or the deletion command of the virtual concatenation member paths issued by the bandwidth set processor."

As set forth in the Examination Guidelines for Determining Obviousness Under 35 U.S.C. §103 in View of the Supreme Court Decision in *KSR* International Co. v. Teleflex Inc. (*KSR*) effective October 10, 2007[Federal Register: October 10, 2007 (Volume 72, Number 195)][Notices][Page 57526-57535]. ("Examination Guidelines"):

> As reiterated by the Supreme Court in KSR, the framework for the objective analysis for determining obviousness under 35 U.S.C. §103 is stated in Graham v. John Deere Co. Obviousness is a question of law based on underlying factual inquiries. . . . (2) Ascertaining the differences between the claimed invention and the prior art; and (3) Resolving the level of ordinary skill in the pertinent art.

(See, Examination Guidelines, page 57527, col. 1).

I. Applicant respectfully submits that the Examiner erred in establishment of the Graham factual inquires. The Examiner asserts Acharya discloses:

> transmission equipment (fig. 6) transmitting traffic input from a plurality of ports on the Synchronous Optical network/Synchronous Digital Hierarchy network paths of which bandwidths are arbitrarily set by Virtual Concatenation and Link capacity Adjustment Scheme.

(Action at page 2, lines 22-25).

The Examiner further relies on Acharya's paragraph [0002] and Fig. 6 as teaching an input traffic collector which collects and retains an input amount of each input port for period at preset periods. (Action at page 2, lines 26 - page 3, line 1).

Applicant submits that the Examiner errs in his interpretation of the teaching of Acharya. Applicant submits that Acharya does not teach in FIG. 6 or elsewhere a collector collecting and retaining an input amount of each input port for period at preset periods, as recited by claim 1.

By contrast, Acharya merely discloses:

> FIG. 6 shows one of the nodes 56-i of network 52 in greater detail. The node 56-i includes a nodal processor 58-i which includes a central processing unit (CPU) and memory. A set of input links 64, corresponding to fiber connections 62 with three other nodes, are connected to buffers 70-1, 70-2 and 70-3 in node 56-i. The node 56-i supplies signals to three other nodes via a set of output links 66 also corresponding to fiber connections 62. The output links 66 are connected to buffers 72-1, 72-2 or 72-3. . . The node 56-i also includes a demand database 76 for storing demands for network capacity, and a set of routing tables which specify routes through the network for particular demands. The demand database 76 and routing tables 77 may be components of a common memory within node 56-i, and may be combined with or otherwise associated with the memory of nodal processor 58-i.

(See, for example, paragraphs [0081] and [0082]).

That is, Acharya does not teach any collecting and retaining at preset periods. Further, Applicant submits Acharya merely teaches (see for example, paragraphs [0003] and [0004]) conventional techniques regarding virtual concatenation and LCAS. The specification of the present application discussed such conventional techniques in the section application entitled "Background of the invention" starting at page 1, line 13 - page 5, line 18.

II. The Action concedes that Acharya does not disclose a bandwidth set processor. (Action at page 3, lines 7-8). However, the Examiner asserts that Sandstrom teaches:

> a bandwidth set processor which calculates a bandwidth for use in each input port from the input traffic amount retained in the input traffic collector, calculates the corresponding number of virtual concatenation member paths from the difference of the bandwidth in use and a virtual concatenation path bandwidth having been allocated to the input port, and issues an addition command or a deletion command for adding or deleting the virtual concatenation member paths for the calculated number . . . it would have been obvious . . . to mount the bandwidth set processor taught by Sandstrom onto the transmission equipment as shown in Acharya, in order to control bandwidth allocation so that the systems run more efficient.

(Action at pate 3, lines 8-19)

Applicant submits that the Examiner also errs in his interpretation of the teaching of Sandstorm and that Sandstorm does not teach a bandwidth set processor that calculates a bandwidth for use in each input port from the traffic amount of traffic signals, retained in the input traffic collector, calculates the corresponding number of virtual concatenation member paths from the difference between the calculated bandwidth in use and a virtual concatenation path bandwidth having been allocated to the input port, and issues an addition command for adding or a deletion command for deleting the virtual concatenation member paths for the calculated number, as recited by claim 1.

By contrast, Sandstrom merely discloses:

> The present invention enables dynamic adjustment of the capacity of SDH/SONET connections by automatically adding and removing Paths to/from the connections formed of virtual-concatenated Paths based on the actual volumes of the packet traffic flows between the access interfaces of the SDH/SONET network and fair sharing of network resources.

(see, for example, col. 2, lines 59-65)

That is, Sandstorm does not teach a bandwidth set processor that calculates a bandwidth for use in each input port from the traffic amount of traffic signals, retained in the input traffic collector,as recited by claim 1. Further, Sandtrom does not teach a bandwidth set processor that caculates the corresponding number of virtual concatenation member paths from the difference between the calculated bandwidth in use and a virtual concatenation path bandwidth having been allocated to the input port.

III. Applicant further submits that according to an embodiment of the invention, as recited by claim 1 may yield unpredictable results or effects such that timings can be determined for adding or deleting virtual concatenation paths arbitrarily by a maintenance operator. In addition, an optimum number of member paths can be added or deleted to correspond to amounts of traffic signals by obtaining the difference between the calculated bandwidth in use and a virtual concatenation path bandwidth having been allocated to the input port.

Summary

Applicant submits that even an *arguendo* combination of the art relied on does not teach all features recited by independent claim 1, and the rejection should be withdrawn and independent claim 1 (and dependent claims 2-5) allowed.

Dependent claims are separately allowable

I. In item 3 of the Office Action, the Examiner rejects dependent claim 2 under 35 U.S.C. §103(a) as being unpatentable over Acharya in view of Sandstrom (U.S.P. 6,697,373). The rejection is traversed.

Dependent claim 2 recites transmission equipment according to claim 1 including "a virtual concatenation information storage which retains correspondence between each destination node of the virtual concatenation member paths and each input port, wherein the bandwidth set processor allocates an idle virtual concatenation member path having not been allocated to any virtual concatenation paths to an input port which has the same destination node and requires increasing the virtual concatenation path bandwidth (emphasis added)."

The Examiner asserts that:

> Sandstrom teaches a virtual concatenation information storage which retains correspondence between each destination node of the virtual concatenation member paths and each input port, wherein the bandwidth set processor allocates an idle virtual concatenation member path having not been allocated to any virtual concatenation paths to an input port which has the same destination node and requires increasing the virtual concatenation path bandwidth . . . it would have been obvious . . . to mount the virtual concatenation information storage taught by Sandstrom onto the transmission' equipment as show in Acharya, in order to manage available bandwidth so that the systems run quicker.

(Action at page 3, starting at line 19 - page 4, line 9).

Applicant submits that the Examiner errs in his interpretation of the teaching of Sandstorm and that Sandstrom does not teach a bandwidth set processor that allocates an idle virtual concatenation member path having not been allocated to any virtual concatenation paths to an input port which has the same destination node and requires increasing the virtual concatenation path bandwidth, as the Examiner asserts. By contrast, Sandstrom merely discloses:

> Paths with matching destination identification are associated in their concatenation groups with their concatenation order, and the virtual-concatenated payloads are recovered. All the Paths between any two PTs belong to the same concatenation group. A Path added to or removed from a certain concatenation group is always the Path with highest concatenation order in that concatenation group.

(see, for example, col. 12, lines 15-19).

That is, neither Sandstrom nor an *arguendo* combination of Sandstrom and Archarya teaches idle virtual concatenation member path having not been allocated to any virtual concatenation paths to an input port which has the same destination node and requires increasing the virtual concatenation path bandwidth.

Summary

Applicant submits that even an *arguendo* combination of the art relied on does not teach all features recited by dependent claim 2 and the rejection should be withdrawn and claim 2 allowed.

II. In item 4 of the Office Action, the Examiner rejects dependent claim 3 under 35 U.S.C. §103(a) as being unpatentable over Acharya in view of combinations of Sandstrom andMacLean (US Pat. App. Pub. No.2005/0073955). The rejection is traversed.

Dependent claim 3 recites transmission equipment including "an input port set information storage which retains a bandwidth allocation priority and a minimum guarantee bandwidth, wherein, in the bandwidth set processor, when the addition command of a virtual

concatenation member path is issued to the link capacity adjustment scheme controller, an input port having a higher priority is processed preferentially, and when the deletion command of a virtual concatenation member path is issued to the link capacity adjustment scheme controller, the issue of the deletion command is restrained so that the virtual concatenation path bandwidth may not fall below the minimum guarantee bandwidth."

The Action concedes that a combination of Acharya and Sandstrom does not disclose a input port information storage with a bandwidth allocation priority and a minimum guarantee bandwidth. (Action at page 4, lines 16-18). However, the Examiner asserts that:

> MacLean teaches an input port set information storage which retains a bandwidth allocation priority and a minimum guarantee bandwidth, (see Page. 3, Paragraph [0020]) wherein, in the bandwidth set processor, (see Page. 2, Paragraph [0018]) when the addition command of a virtual concatenation member path is issued to the link capacity adjustment scheme controller, an input port having a higher priority is processed preferentially, (see Page. 2, Paragraph [0013]) and when the deletion command of a virtual concatenation member path is issued to the link capacity adjustment scheme controller, the issue of the deletion command is restrained so that the virtual concatenation path bandwidth may not fall below the minimum guarantee bandwidth (see Page. 1, Paragraph [0005] and see Page. 3, Paragraph [0021]) . . . .it would have been obvious . . . to mount the input port information storage with a bandwidth allocation priority and a minimum guarantee bandwidth taught by MacLean onto the transmission equipment as show in the system of Acharya, and Sandstrom in order to provide the minimum bandwidth and operate bandwidth priority so that the systems run more efficient.

(Action at page 4, line, 19 - page 5, line 11).

Applicant submits that the Examiner errs in his interpretation of the teaching of MacLean and that neither MacLean nor an *arguendo* combination of the art relied on teaches "any input port set information storage which retains a bandwidth allocation priority and minimum guarantee bandwidth," as recited by claim 3. By contrast, MacLean merely teaches:

> The base bandwidth parameter determines the minimum bandwidth to be given the service over the path. The value assigned to this parameter ensures that the service always has bandwidth available, even on links that are used to their bandwidth capacity. Accordingly, the base bandwidth for each service is at least one STS-1.

(see, for example, paragraph 0020)

That is, MacLean merely teaches a base bandwidth parameter determines the minimum bandwidth to be given the service over the path, but fails to teach any allocation priority, and does not teach "any input port set information storage which retains a bandwidth allocation priority and minimum guarantee bandwidth".

Summary

Applicant submits that even an *arguendo* combination of the art relied on does not teach

all features recited by dependent claim 3 and the rejection should be withdrawn and dependent claim 3 allowed.

III. In item 5 of the Office Action the Examiner rejects dependent claim 4 under 35 U.S.C. §103(a) as being unpatentable over Acharya in view of combinations of Sandstrom and Kfir (U.S. Pat. App.Pub. No. 2004/0076176). The rejection is traversed.

Dependent claim 4 recites transmission equipment including "buffers each of which retains the input traffic correspondingly to each of the plurality of input ports, wherein, the preset period for collecting the input traffic amount in the input traffic amount collector is determined by calculating ratios of each buffer size to each maximum bandwidth for the entire plurality of input ports, and using the shortest value as the preset period."

The Action concedes that a combination of Acharya and Sandstrom does not teach "to use a buffer to control input traffic." (Action at page 5, lines 17-18). However, the Examiner asserts that Kfir teaches:

> buffers (fig.1) each of which retains the input traffic correspondingly to each plurality of input ports, wherein, the preset period for collecting the input traffic amount in the input traffic amount collector is determined by calculating ratios of each buffer size to each maximum bandwidth for the entire plurality of input ports, and using the shortest value as the preset period (see Page. 4, Paragraph [0061]). . . .obvious to . . . incorporate the buffer taught by Kfir into the transmission equipment as show in the system of Acharya, and Sandstrom in order to save the data so that the systems become well organized.

(Action at page 5, line 18 - page 6, line 6).

By contrast, Kfir merely teaches:

> Preferably, the synchronous processor 55 includes at least one buffer 75 that receives and arranges electronic signals for processing by synchronous processor 55 and/or for transmitting either to the network terminal associated with NE 20 or to the transceiver sections in nodes 48 in the synchronous infrastructure 15. The at least one buffer 75 is clocked by clock 80, and both clock 80 and the at least one buffer 75, as well as the synchronous processor 55, may preferably be controlled by controller 60, for example, according to management information received from the network management system 30.

(see, for example, paragraph [0061]).

Applicant submits that neither Kfir, nor an *arguendo* combination of the art relied on by the Examiner teaches that the "at least one buffer" disclosed by Kfir "retains the input traffic correspondingly to each of the plurality of input ports, wherein, the preset period for collecting the input traffic amount in the input traffic amount collector is determined by calculating ratios of each buffer size to each maximum bandwidth for the entire plurality of input ports, and using the shortest value as the preset period, (emphasis added), as recited by claim 4."

Summary

Applicant submits that even an *arguendo* combination of the art relied on does not teach all features recited by dependent claim 4 and the rejection should be withdrawn and dependent claim 4 allowed.

IV. In item 6 of the Office Action, the Examiner rejects dependent claim 5 under 35 U.S.C. §103 (a) as being unpatentable over Acharya in view of combinations of Sandstrom and ATRICA "Migration from SONET/SDH to Carrier Ethernet In Metropolitan Area" ("Atrica"). The rejection is traversed.

Dependent claim 5 recites equipment "wherein, when the input port bandwidth in use falls below the virtual concatenation path bandwidth, the bandwidth set processor suspends issue of the deletion command of a virtual concatenation member path to the link capacity adjustment scheme controller for a certain time, thereby avoiding a state of failure to establish the virtual concatenation required for transmission, caused by excessive addition or deletion of the virtual concatenation member paths in the link capacity adjustment scheme in case of unstable input traffic amount."

The Action concedes that Acharya and Sandstrom do not teach "how to control underflow, where in underflow, is defined as the input port bandwidth, which falls below the virtual concatenation path bandwidth." (Action at page 6, lines 12-14). However, the Examiner asserts that Atrica teaches:

> when the input port bandwidth in use falls below the virtual concatenation path bandwidth, the bandwidth set processor suspends issue of the deletion command of a virtual concatenation member path to the link capacity adjustment scheme controller for a certain time, thereby avoiding a state of failure to establish the virtual concatenation required for transmission, caused by excessive addition or deletion of the virtual concatenation member paths in the link capacity adjustment scheme in case of unstable input traffic amount (page 11, citation 3.2.3 paragraph 2)... obvious . . . to control underflow in a way taught by Atrica in the transmission equipment as shown in the system of Acharya, and Sandstrom, in order to save the extra bandwidth so that the systems become cost efficient.

(Action at page 6, line 14 - page 7, line 4).

Applicant submits that the Examiner errs in his interpretation of the teaching of Atrica and that neither Atrica nor an *arguendo* combination of the art relied on, when the input port bandwidth in use falls below the virtual concatenation path bandwidth, the bandwidth set processor suspends issue of the deletion command of a virtual concatenation member path to the link capacity adjustment scheme controller for a certain time, thereby avoiding a state of failure to establish the virtual concatenation required for transmission, caused by excessive

addition or deletion of the virtual concatenation member paths in the link capacity adjustment scheme in case of unstable input traffic amount. By contrast, Atrica merely teaches:

> LCAS is an ITU-standard signaling scheme that allows two endpoints of a VC channel to tune the bandwidth dynamically at the request of the network management system without disturbing traffic. VCAT can be used without LCAS, however LCAS requires VCAT support. This is because the LCAS control commands share H4 bytes with VCAT MFI and SQ, and LCAS needs to assign SQ to the newly added sub-channel and sets other control commands such as EOS (End of Sequence) or NORM (Normal Operating Mode) in H4 bytes of POH. A likely misunderstanding of LCAS is that LCAS allows SONET/SDH to tune a VCAT channel automatically according to the traffic rate. But in fact the network management system needs to send a command to the source node for adding/deleting a sub-channel to/from the existing VCAT channel. The source node uses LCAS commands to notify the destination node of the addition/deletion of the sub-channel.

(See, for example, 3.2.3).

Summary

Applicant submits that even an *arguendo* combination of the art relied on does not teach all features recited by dependent claim 5 and the rejection should be withdrawn and dependent claim 5 allowed.

New claims

New claims 6-7 recite features of the present invention in a different fashion. New claim 6 recites an input traffic collector for transmission equipment including "a collector which collects and retains a traffic amount of traffic signals input in each input port for one period at preset periods; and buffers each of which retains the input traffic correspondingly to each of the plurality of input ports, wherein, the preset period for collecting the input traffic amount in the collector is determined by calculating ratios of each buffer size to each maximum bandwidth for the entire plurality of input ports, and using the shortest value as the preset period."

New claim 7 recites bandwidth set processor including "a processor that calculates a bandwidth for use in each input port from traffic amount of traffic signals, calculates a corresponding number of virtual concatenation member paths from a difference between the calculated bandwidth in use and a virtual concatenation path bandwidth having been allocated to the input port, and issues an addition command for adding or a deletion command for deleting the virtual concatenation member paths for the calculated number; and a link capacity adjustment scheme controller which controls a virtual concatenation to set and change the virtual concatenation path bandwidth, based on the addition command or the deletion command of the virtual concatenation member paths issued by the bandwidth set processor, wherein, when the input port bandwidth in use falls below the virtual concatenation path bandwidth, the

bandwidth set processor suspends issue of the deletion command of a virtual concatenation member path to the link capacity adjustment scheme controller for a certain time."

Support for the new claims is found, for example, on page 14, line 15 - page 16, line 20. paragraphs. No new matter is being presented, and approval and entry are respectfully requested.

These, and other, features of claims 6-7 patentably distinguish over the cited art, and they are submitted to be allowable for the recitations therein.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is invited to telephone the undersigned to attend to these matters.

Please charge any fees associated with filing this Amendment to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: December 6, 2007

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